UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,368	11/19/2003	David Walter Flynn	550-489	9185

23117 7590 08/24/2007

NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
BROWN, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2116	
MAIL DATE	**DELIVERY MODE**
08/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

mN

Office Action Summary	Application No.	Applicant(s)	
	10/715,368	FLYNN, DAVID WALTER	
	Examiner	Art Unit	
	Michael J. Brown	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)* Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cooper(US Patent 6,823,516) in view of Kobayashi et al.(US Patent 6,148,415).

As to claim 1, Cooper discloses an apparatus(system 10, see Fig. 1) for processing data, said apparatus comprising a processor(processor 12, see Fig 1) operable to perform data processing operations, said processor being operable to generate a performance control signal indicative of a desired data processing

performance level of said processor(see column 3, lines 19-27), and at least one further circuit(performance control logic 16, see Fig. 1) responsive to said performance control signal to support said desired data processing performance level of said processor(see column 5, lines 24-27). Cooper also discloses the apparatus wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level(low power state, see column 5, lines 35-36) to a second desired data processing performance level(high power state, see column 5, line 36), and said processor temporarily operates at said at least one intermediate data processing performance level during said change(see column 5, lines 33-42 and column 8, lines 6-9). However, Cooper fails to disclose the at least one further circuit supports data processing of the processor at at least one intermediate data processing performance level.

Kobayashi teaches at least one further circuit(backup data processor 101, see Fig. 1) supports data processing of a processor at at least one intermediate data processing performance level("event that the processor 1 develops a failure", see column 3, line 46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to add Kobayashi's backup data processor to Cooper's system for adjusting CPU performance changes in order to maintain data processing capabilities during the temporary downtime of the main processor. The motivation to do so would be to assure that data being processed and data concerning the failure are dumped to an auxiliary memory to facilitate analysis of the failure(see Kobayashi Abstract, lines 16-18).

As to claim 2, Cooper discloses the apparatus wherein said one or more further circuits include a voltage controller operable to generate a power signal for said processor at a plurality of different voltage levels(see column 4, lines 56-61).

As to claim 3, Cooper discloses the apparatus wherein said one or more further circuits include a clock generator operable to generate a clock signal with a selectable clock frequency(see column 3, lines 52-60).

As to claim 4, Cooper discloses the apparatus wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency to an intermediate clock signal frequency when said voltage controller is generating a power signal with a voltage level sufficient to support said intermediate clock signal frequency(see column 4, lines 15-34).

As to claim 5, Cooper discloses the apparatus wherein one or more priority signals(IGGNE#, A20M#, LINTO#, and LINT1#, see column 4, line 20) serve to trigger said further circuit change to support a predetermined data processing performance level independently of said performance control signal(see column 4, lines 17-21).

As to claim 6, Cooper discloses a method of processing data, said method comprising the steps of performing data processing operations with a processor(processor 12, see Fig 1), said processor being operable to generate a performance control signal indicative of a desired data processing performance level of said processor(see column 3, lines 19-27), and in response to said performance control signal, operating one or more further circuits(performance control logic 16, see Fig. 1) so as to support said desired data processing performance level of said processor(see

column 5, lines 24-27). Cooper also discloses the method wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level(low power state, see column 5, lines 35-36) to a second desired data processing performance level(high power state, see column 5, line 36), said operating step includes supporting data processing at at least one intermediate data processing performance level(see "time it takes to switch between performance states", column 8, lines 8-9) and said processor temporarily operates at said at least one intermediate data processing performance level during said change(see column 5, lines 33-42 and column 8, lines 6-9). However, Cooper fails to disclose said operating step includes supporting data processing of the processor at at least one intermediate data processing performance level.

Kobayashi teaches an operating step(operation of backup data processor 101, see Fig. 1) includes supporting data processing of a processor at at least one intermediate data processing performance level("event that the processor 1 develops a failure", see column 3, line 46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to add Kobayashi's backup data processor to Cooper's system for adjusting CPU performance changes in order to maintain data processing capabilities during the temporary downtime of the main processor. The motivation to do so would be to assure that data being processed and data concerning the failure are dumped to an auxiliary memory to facilitate analysis of the failure(see Kobayashi Abstract, lines 16-18).

As to claim 7, Cooper discloses the method wherein said one or more further circuits include a voltage controller operable to generate a power signal for said processor at a plurality of different voltage levels(see column 4, lines 56-61).

As to claim 8, Cooper discloses the method wherein said one or more further circuits include a clock generator operable to generate a clock signal with a selectable clock frequency(see column 3, lines 52-60).

As to claim 9, Cooper discloses the method wherein, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency to an intermediate clock signal frequency when said voltage controller is generating a power signal with a voltage level sufficient to support said intermediate clock signal frequency(see column 4, lines 15-34).

As to claim 10, Cooper discloses the method wherein one or more priority signals(IGGNE#, A20M#, LINTO#, and LINT1#, see column 4, line 20) serve to trigger said further circuit change to support a predetermined data processing performance level independently of said performance control signal(see column 4, lines 17-21).

As to claim 11, Cooper an apparatus(system 10, see Fig. 1) for processing data, said apparatus comprising a processor(processor 12, see Fig 1) operable to perform data processing operations, said processor being operable to generate a performance control signal indicative of a desired data processing performance level of said processor(see column 3, lines 19-27), and at least one further circuit(performance control logic 16, see Fig. 1), responsive to said performance control signal, for supporting said desired data processing performance level of said processor(see

column 5, lines 24-27). Cooper also discloses the apparatus wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level(low power state, see column 5, lines 35-36) to a second desired data processing performance level(high power state, see column 5, line 36), said at least one further circuit comprising a means for supporting data processing at at least one intermediate data processing performance level(see "time it takes to switch between performance states", column 8, lines 8-9) and said processor temporarily operates at said at least one intermediate data processing performance level during said change(see column 5, lines 33-42 and column 8, lines 6-9). However, Cooper fails to disclose the at least one further circuit comprising means for supporting data processing of the processor at at least one intermediate data processing performance level.

Kobayashi teaches at least one further circuit(backup data processor 101, see Fig. 1) comprising means for supporting data processing of a processor at at least one intermediate data processing performance level("event that the processor 1 develops a failure", see column 3, line 46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to add Kobayashi's backup data processor to Cooper's system for adjusting CPU performance changes in order to maintain data processing capabilities during the temporary downtime of the main processor. The motivation to do so would be to assure that data being processed and data concerning the failure are dumped to an auxiliary memory to facilitate analysis of the failure(see Kobayashi Abstract, lines 16-18).

Response to Arguments

2. Applicant's arguments filed 6/18/2007 have been fully considered but they are not persuasive. Applicant argues that neither Cooper not Kobayashi disclose the at least one further circuit supports data processing of the processor the processor temporarily operating at the at least one intermediate data processing performance level during said change. Examiner disagrees as Kobayashi teaches that in the event that the processor develops a failure, disconnecting the processor, thus making it inoperable(intermediate data processing performance level), and the backup data processor 101 then supports data processing(see column 3, lines 45-55). Under the current claim language Cooper in view of Kobayashi satisfies the claim in that the processor is temporarily operating at at least one intermediate data processing level(disconnected, thus inoperable) during the change.

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Brown whose telephone number is (571)272-5932. The examiner can normally be reached Monday-Thursday from 7:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571)272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
8/24/07

Michael J. Brown
Art Unit 2116